REMARKS

Favorable reconsideration of this application, as amended, is respectfully requested.

The Examiner's indication of allowable subject matter in various claims is noted with appreciation.

Applicants also appreciate the Examiner's acknowledgement of the Applicants' claim for foreign priority under 35 U.S.C. § 119(a) and receipt of the certified priority document, and the Examiner's provision of an endorsed copy of the Form PTO-1449 filed in connection with this application.

The specification has been amended to delete references to Fig. 4 and to add references to Figs. 4a and 4b.

Claims 1 and 2 have been amended to address the objection to the phrase "applying them". With respect to the remaining objections, the Applicants note that the alleged deficiencies do not appear in the claims submitted in the Preliminary Amendment dated November 5, 2003, and therefore the objection may not be fairly maintained (see the scanned claims in PAIR). Accordingly, withdrawal of this objection is respectfully requested.

Claims 2-3 and 8-11 have been editorially revised to improve clarity without affecting their allowability. Claims 12 and 13 have been added, dependent from Claim 1.

Further, without acceding to the outstanding rejection under 35 U.S.C. § 102(b), independent Claim 1 has been amended more particularly to recite the control operation of the control unit. Specifically, Claim 1 has been amended to recite that the control unit performs control such that in the erase operation a lower erase voltage is applied to a control gate of each of the nonvolatile memory cells and thereafter a higher erase voltage is applied to the control gate of each of the nonvolatile memory cells.

At least as presently amended, Claim 1 distinguishes patentably from the Haddad et al. reference (Haddad), which constitutes the basis for the aforementioned rejection. Specifically, Haddad discloses that selected memory cells of a flash EEPROM array are erased by applying a relatively high negative voltage (i.e., -12V to -17V) to a control gate electrode of each cell (see Haddad, Col.3, lines 40-43). In Haddad, the range "-12 to -17" does not represent multiple voltage applications. Rather, the range "-12 to -17" indicates a range within which the (single) applied "relatively high" voltage may reside.

In contrast to Applicants' invention as now set forth in Claim 1, a lower erase voltage of Haddad is not applied to a control gate before applying a relatively

high voltage to the control gate, both in one erase operation. Accordingly, independent Claim 1, and its dependents, should now be allowed.

An early Notice of Allowance is respectfully solicited.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on May 10, 2005.

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Mitchell W. Shapiro